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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,602	11/14/2001	Wingyu Leung	MST-012	4719

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EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,602	LEUNG ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/01; 4/13/04;* 02/04/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Application Serial No: 10/003,602

Claim Rejections - 35 USC § 112

1. Claims 4-5, 7-12, 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4:

At line 4, it is not clear when and how "a (new) write address value applied to the first register"? What is the difference between the write address value (as being recited at line 4) and "the write address value" as being recited at line 3?

Claim 7 (depends on claim 1):

It is not clear whether the term "a write data value" at line 3 and the term "a write address value" at lines 3-4 refer to any of the previously recited write data value and previously recited write address value in claim 1.

At line 5, it is not clear whether the term "a write data value" refers to the previously recited "a write data value" at line 3.

At lines 7-8, it is not clear whether the term "a write address value" refers to the previously recited "a write address value" at lines 3-4.

At line 5, the phrase "means for retiring ... to a location in the memory array" cannot be understood due to wrong of use of a word "retiring". The word "retire/retiring" means "withdraw/withdrawing" in a WEBSTER's II Dictionary.

Claim 8:

At line 13, the phrase "means for retiring ... to a location in the memory array" cannot be understood due to wrong of use of a word "retiring". The word "retire/retiring" means "withdraw/withdrawing" in a WEBSTER's II Dictionary.

Claim 9:

At line 6, the phrase "means for retiring ... to a location in the memory array" cannot be understood due to wrong of use of a word "retiring". The word "retire/retiring" means "withdraw/withdrawing" in a WEBSTER's II Dictionary.

Claim 20:

At line 13, the phrase "means for retiring ... to a location in the memory array" cannot be understood due to wrong of use of a word "retiring". The word "retire/retiring" means "withdraw/withdrawing" in a WEBSTER's II Dictionary.

It is not clear whether or not the terms "a plurality of data/ECC values" at line 23, "a data value" at lines 24-25, "a corresponding ECC value" at line 25 refer to any of the previously recited first write data value, second write data value, first ECC value, or second ECC value. In other words, consistency of terms should be used through out a claim.

It is not clear whether or not the terms "a first data/ECC value" (at line 27) and "a first address" (at lines 27-28) refers to the previously recited first data/ECC value (at line 23) and the previously recited first address (at line 4).

Claims 5, 10-12:

These claims are rejected because they depend on claims 4 and 8 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-10, 13-15, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales et al (6,101,614 and Gonzales hereinafter).

Claims 1, 2:

Gonzales discloses the invention substantially as claimed. Gonzales teaches (figures 1-3) a computer system comprising a memory controller (MC) for handling memory access requests and memory interface components (MICs) for interfacing the MC to a memory array. The MC is divided into separate components naming as a DRAM controller (DC) and a data path (DP). When writing data, data is first popped off to a write data buffer (in the DP) and then input to the ECC code word generation unit where 8 parity bits are calculated and appended to the DWORD to form a 72 bit code where that is subsequently written to the memory array (figures 1, 2 and 3, column 4 lines 14-23 and 54-62, column 6 lines 60-67).

Gonzales does not explicitly teach that the write buffer also receive and store a write address value. However, Gonzales teaches that the DRAM controller (DC) is consisted of a queue management unit (QMUC) for buffering addresses received from a

bus engine (BEC) into a memory interface (MMIC) (column 5 lines 21-25, column 5 lines 38-44).

It would have been obvious to one skilled in the art at the time the invention was made to combine both Gonzales' write data buffer and Gonzales' QMUC together for storing both the data and the corresponding addresses. The artisan would have been motivated to do so because Gonzales suggests not only the MC can divided into separate components (DC and DP), but also can be implemented as a single package (column 5 lines 2-8).

Claim 3:

Gonzales's MIO buffers store the 72-bit DWORD (data appended with parity bits) to be written to the memory (column 6 lines 62-67). Gonzales also teaches the MMIC for storing address ADDR to be sent to the memory (figure 2, column 5 lines 38-44).

Claim 6:

Gonzales teaches that each set of data buffer comprises four buffers, any number of read and write data buffers may be used in a pipelined system (column 6 lines 11-15).

Claim 7:

Gonzales teaches that a set of write data buffers (in the QMUD) temporarily buffers write data received from the system bus before it is written to the memory. Such set of buffers may be used in a pipelined system such that a total of eight different memory access may be in process at one time (column 6 lines 4-16).

Claims 8 and 9:

Claims 8 and 9 rejected for reasons similar to those set forth against claims 1, 6 and 7.

Claim 10:

Gonzales does not explicitly teach the enabling tri-state buffers during the write access. Gonzales, however, teaches a set of four data buffers for buffering write data received from the system bus before it is written to the memory wherein the buffers are used in a pipelined system (column 6 lines 4-16). It would have been obvious to one skilled in the art at the time the invention was made to use the tri-state buffers. The artisan would have been motivated to do so because (1) tri-state buffers are well-known in the art, and (2) Gonzales's write data buffers do not exclude from the inclusion of tri-state buffers.

Claim 13:

Gonzales shows (figures 1-3) a method and apparatus for scrubbing ECC errors in memory upon detecting correctable errors in data read from memory through the use of a writeback path coupled between the outputs of the read and write data buffer of a memory controller. Gonzales teaches that read data in the form of a 72-bit code word is first buffered in the MIO buffers and then directed into the ECC checking and correcting unit to decode the code word. If an error did occur, the ECC checking and correcting unit sends this error condition signal to report to the MCL of the DC

component via an error bus. The ECC checking and correcting unit also corrects data and then sends it to the next allocated read buffer in the QMUD. The MCL then issues the appropriate address and request attribute signals to both the MICs and the memory array via a memory control bus so that the corrected data is then written to the location in memory specified by the original read request still present in the request queue of the DC component (figure 3, column 7 lines 1-16, 46-50; column 8 lines 23-33).

Gonzales does not explicitly teach the write-back buffer. However, Gonzales suggests the read data buffers in the QMUD such one of the read data buffers stores the corrected data and then sends the corrected data back to the memory (column 7 lines 46-50, column 8 lines 23-33). It would have been obvious to one skilled in the art at the time the invention was made to name Gonzales's read data buffer as "write-back buffer". The artisan would have been motivated to do so because naming Gonzales's read data buffer as "write-back buffer" would not affect the performance of the read data buffer.

Claims 14 and 15:

Gonzales's write data buffers may be used in either a pipelined or non-pipelined system without departing from the spirit of his invention (column 6 lines 14-15).

Claim 17:

Due to the similarity of claim 17 to claim 13, this claim is also rejected under the same rationale applied against claim 13.

Claim 18:

Gonzales teaches that to maximize system performance in a pipelined system, a set of write data buffers (in the QMUD) comprises four buffers such that a total of eight different memory access may be in process at any one time (column 6 lines 4-14).

Claims 19 and 20:

Claims 19 and 20 are rejected for reasons similar to those set forth against claims (1 & 13) and (8 & 17), respectively.

4. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2133

August 7, 2004